SEMICONDUCTOR INTEGRATED CIRCUIT AND IMAGE SENSOR

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-169679; filed August 28, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor integrated circuit and an image sensor.

BACKGROUND

A voltage value which is read from a pixel of an image sensor is converted into a digital signal by an AD converter which is provided in each column. A single slope type AD converter (hereinafter, referred to as SSADC) with a small area is frequently used for the AD converter. In the SSADC, the greater the slope of a ramp voltage is, the wider a dynamic range is, but noise increases.

An example of related art includes JP-A-2014-75847.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a schematic configuration of an image sensor according to a first embodiment.

FIG. 2 is a circuit diagram illustrating an example of an internal configuration of a pixel.

FIG. 3 is a circuit diagram illustrating a configuration of a signal conversion unit.

FIGS. 4A and 4B illustrate coupling states of a signal conversion unit in each operation step.

FIGS. 5A and 5B illustrate coupling states of the signal conversion unit in each operation step.

FIGS. 6A and 6B illustrate coupling states of the signal conversion unit in each operation step.

FIG. 7 is a timing diagram of a voltage Vpix and a third voltage Vx at the time of an AD conversion operation.

FIG. 8 is a timing diagram of the voltage Vpix and the third voltage Vx at the time of an AD conversion operation.

FIG. 9 is a block diagram illustrating a configuration of an output unit.

FIGS. 10A and 10B illustrate coupling states of a signal conversion unit in each operation step at the time of measuring an offset code between first capacitors.

FIG. 11 illustrates a coupling state of a signal conversion unit in each operation step at the time of measuring an offset code between the first capacitors.

FIG. 12 is a timing diagram of the voltage Vpix and the third voltage Vx at the time of an AD conversion operation corresponding to FIGS. 10A to 11.

FIG. 13 is a flow chart illustrating processing in which an offset code that is generated by each first capacitor is obtained.

FIG. 14A is a circuit diagram of an essential part of an AD converter according to a first comparison example, and FIG. 14B is a timing diagram of the AD converter.

FIG. 15A is a circuit diagram of an essential part of an AD converter according to a second comparison example, and FIG. 15B is a timing diagram of the AD converter.

FIG. 16A is a diagram illustrating noise of the second comparison example, and FIG. 16B is a diagram illustrating noise of a first embodiment.

FIG. 17 is a circuit diagram illustrating a configuration of a signal conversion unit according to a second embodiment.

FIG. 18 is a circuit diagram illustrating a configuration of a signal conversion unit according to a third embodiment.

FIG. 19 is a timing diagram of a voltage Vpix and a third voltage Vx at the time of an AD conversion operation.

FIG. 20A illustrates a correspondence relationship between a second digital signal, the number of generations, and the amount of shifted bits, and FIG. 20B illustrates an example of the shifted bits in a case of M=2.

FIG. 21 is a circuit diagram illustrating a configuration of a signal conversion unit according to a fourth embodiment.

FIGS. 22A and 22B illustrate coupling states of a signal conversion unit in each operation step of a single slope AD conversion.

FIGS. 23A and 23B illustrate coupling states of a signal conversion unit in each operation step of a single slope AD conversion.

FIG. 24 is a timing diagram of a voltage Vpix and a third voltage Vx at the time of an AD conversion operation.

FIG. 25 illustrates a correspondence relationship between a second digital signal, the number of generations, and the amount of shifted bits.

FIG. 26 illustrates a relationship between the amount of a third voltage Vx shifted by a unit capacitor and the amount of the third voltage Vx changed by 1 LSB of a second digital signal.

FIG. 27 is a circuit diagram illustrating a configuration of a signal conversion unit according to a fifth embodiment.

FIG. 28 is a timing diagram of a voltage Vpix and a third voltage Vx at the time of an AD conversion operation.

FIG. 29 illustrates a relationship between the amount of a third voltage Vx shifted by a third capacitor and the amount of the third voltage Vx changed by 1 LSB of a second digital signal.

DETAILED DESCRIPTION

[0004]is the embodiments provide a semiconductor integrated circuit and an image sensor which can perform an AD conversion at a small area, a wide dynamic range, and low noise.

[0005]In general, according to one embodiment, a semiconductor integrated circuit includes a comparator, a capacitor unit having a plurality of first capacitors, a second capacitor, a switch, and a digital signal generation unit. The comparator includes a first input node to which a first voltage or a second voltage is supplied, a second input node to which a third voltage is supplied, and an output node, and outputs a comparison result which is obtained by comparing the first voltage or the second voltage to the third voltage from the output node. The plurality of first capacitors respectively have one terminal which is coupled to the second input node, and the other terminal to which a first reference voltage or a second reference voltage is supplied. The second capacitor includes one terminal to which a third reference voltage or a ramp voltage is supplied, and the other terminal which is coupled to the second input node. The switch is coupled between the second input node and the output node. The digital signal generation unit generates a first digital signal based on the comparison result.

[0007]Hereinafter, embodiments will be described with reference to the drawings. The embodiments do not limit the disclosure.

First Embodiment

[0008]FIG. 1 is a block diagram illustrating a schematic configuration of an image sensor according to a first embodiment. The image sensor includes a plurality of pixels 1, a row decoder 2, a signal conversion unit 3, and an output unit 4. At least a portion of those can be embedded as a semiconductor integrated circuit.

[0009]The pixels 1 are disposed in a matrix form. The number of pixels in a horizontal (column) direction is referred to as n, and the number of pixels in a vertical (row) direction is referred to as m. Each pixel 1 generates a voltage Vpix corresponding to intensity of light which is incident. Then, the pixel in a kth column outputs the generated voltage Vpix to a signal line Vpix(k) (k is 0 to (n-1)). Hereinafter, the signal “Vpix(k)” or the like is used as the name of a signal line (or terminal), and is also used as a voltage value of the signal line (or the terminal).

[0010]Since the pixel 1 performs so-called correlated double sampling (CDS), the pixel 1 generates a voltage Vpix (hereinafter, referred to as reset voltage (first voltage) Vrst) in a case in which light is not incident, and a voltage Vpix (hereinafter, referred to as a signal voltage (second voltage) Vsig).

[0011]The row decoder 2 sequentially selects one of m rows. By doing so, the voltages Vpix(k) which are generated by n pixels in the selected row are respectively output to the signal lines Vpix(k).

[0012]One signal conversion unit 3 is disposed for one row of pixels, and a total of n signal conversion units 3 is disposed. In other words, the signal conversion units 3(0) to 3(n-1) are provided in correspondence with the signal lines Vpix(0) to Vpix(n-1). The signal conversion unit 3(k) converts the reset voltage Vrst and the signal voltage Vsig, which are read from the pixel 1, into a second digital signal Dout\_m(k) and a fifth digital signal Dout\_l(k).

[0013]The output unit 4 outputs a first digital signal Dout, based on the second digital signal Dout\_m(k) and the fifth digital signal Dout\_l(k).

[0014]The signal conversion unit 3 and the output unit 4 operate as an AD converter, and convert a difference between the reset voltage Vrst and the signal voltage Vsig into a first digital signal Dout for each pixel.

[0015]FIG. 2 is a circuit diagram illustrating an example of an internal configuration of the pixel 1. The circuit diagram illustrated in FIG. 2 is a just an example, and may be modified in various types.

[0016]The pixel 1 includes nMOS transistors Qn1 to Qn4, and a photo diode PD which performs an electro-optical conversion. The transistor Qn1 has a drain which is coupled to a power supply terminal Vdd, a gate to which a reset signal RESET is input, and a source which is coupled to a floating diffusion FD. The transistor Qn2 has a drain which is coupled to the floating diffusion FD, a gate to which a read signal READ is input, and a source which is coupled to a cathode of the photo diode PD. An anode of the photo diode PD is coupled to a ground terminal.

[0017]The transistor Qn3 has a drain which is coupled to the power supply terminal Vdd, a gate which is coupled to the floating diffusion FD, and a source which is coupled to a drain of the transistor Qn4. The transistor Qn4 has a gate to which an address signal ADD is input, and a source from which the voltage Vpix is output. A source of the transistor Qn4 is coupled to the signal line Vpix(k), and the voltage Vpix is output to the signal line Vpix(k).

[0018]The address signal ADD, the reset signal RESET, and the read signal READ are generated, for example, by the row decoder 2.

[0019]The pixel 1 operates as follows, and generates a reset voltage Vrst and a signal voltage Vsig.

[0020]First, the reset signal RESET is set to a high level. By doing so, the transistor Qn1 is turned on, and the floating diffusion FD is initialized to a predetermined voltage. Thereafter, the reset signal RESET is set to a low level. Here, if the address signal ADD is set to a high level, the transistor Qn4 is turned on. By doing so, the reset voltage Vrst according to a voltage of the floating diffusion FD is output to the signal line Vpix(k).

[0021]In order to generate the signal voltage Vsig, the read signal READ is set to a high level, in a state in which the pixel 1 is irradiated with light. By doing so, the transistor Qn2 is turned on. A current according to intensity (brightness) of light which is applied to the photo diode PD flows through the photo diode PD. The stronger the intensity of light is, the more current flows. The stronger the intensity of light is, the lower a voltage of the floating diffusion FD is. Thereafter, the read signal READ is set to a low level. Here, if the address signal ADD is set to a high level, the signal voltage Vsig according to the voltage of the floating diffusion FD is output to the signal line Vpix(k).

[0022]FIG. 3 is a circuit diagram illustrating a configuration of the signal conversion unit 3(k). The signal conversion unit 3(k) includes comparators 11 and 12, a capacitor 13, a capacitor unit 14, a second capacitor 15, switches RST1 and RST2, an edge detector 16, a first control unit 17, and a second control unit 18.

[0023]The comparator 11 includes a non-inverting input node (first input node) 11a, an inverting input node (second input node) 11b, an inverting output node 11c, and a non-inverting output node 11d. The comparator 11 compares a voltage of the non-inverting input node 11a to a third voltage Vx of the inverting input node 11b, and outputs the comparison result from the inverting output node 11c and the non-inverting output node 11d. The reset voltage Vrst or the signal voltage Vsig is applied to the non-inverting input node 11a as the voltage Vpix.

[0024]The comparator 12 compares the comparison result which is supplied from the inverting output node 11c to an inverting input node 12a through the capacitor 13, to the comparison result which is supplied from the non-inverting output node 11d to a non-inverting input node 12b, and outputs a comparison result Compo from an output node thereof. The comparison result Compo is the same as that of the non-inverting output node 11d of the comparator 11.

[0025]The switch RST1 is coupled between the inverting input node 11b and the non-inverting output node 11d. The switch RST2 is coupled between the inverting input node 12a and the output node of the comparator 12.

[0026]The comparator 12, the capacitor 13, and the switch RST2 may not be provided. In this case, the comparator 11 does not have the inverting output node 11c, the comparison result Compo is output from the non-inverting output node 11d.

[0027]The capacitor unit 14 includes first capacitors 21 to 23, and switches S1 to S6. The capacitor unit 14 switches the switches S1 to S6 in accordance with a second digital signal D of 3 bits, and supplies a first reference voltage Vref1 or a second reference voltage Vref2 to the respective first capacitors 21 to 23.

[0028]Here, the second digital signal D of 3 bits will be described as an example, but the second digital signal D may have a plurality of bits. The number of the first capacitors is the same as the number of bits of the second digital signal D, and the number of the switches is double the number of the first capacitors.

[0029]The first capacitors 21 to 23 respectively include one terminal coupled to the inverting input node 11b and the other terminal to which the first reference voltage Vref1 or the second reference voltage Vref2 is supplied. The first reference voltage Vref1 is higher than the second reference voltage Vref2.

[0030]Capacitance values of the first capacitors 21 to 23 are weighted to a product of 2 of a unit capacitance value C and a power of 2. The capacitance value of the first capacitor 21 is C, the capacitance value of the first capacitor 22 is 2C, and the capacitance value of the first capacitor 23 is 4C.

[0031]Each of the switches S1, S3, and S5 include one terminal coupled to the other terminal of a corresponding first capacitor, and the other terminal to which the first reference voltage Vref1 is supplied.

[0032]Each of the switches S2, S4, and S6 include one terminal coupled to the other terminal of a corresponding first capacitor, and the other terminal to which the second reference voltage Vref2 is supplied.

[0033]The switches S1 and S2 are controlled by the first bit (least significant bit) D[0] of the second digital signal D. The switches S3 and S4 are controlled by the second bit D[1] of the second digital signal D. The switches S5 and S6 are controlled by the third bit (most significant bit) D[2] of the second digital signal D.

[0034]By the configuration, the third voltage Vx is changed in accordance with the second digital signal D. That is, the capacitor unit 14 is configured as a DAC of a capacitor type.

[0035]The second capacitor 15 has one terminal to which a third reference voltage Vramp0 or a ramp voltage Vramp is supplied, and the other terminal which is coupled to the inverting input node 11b. The ramp voltage Vramp increases or decreases as time passes. A capacitance value of the second capacitor 15 is C.

[0036]The edge detector 16 detects a rising edge or a falling edge of the comparison result Compo, and switches a voltage level of an output signal to a high level or a low level.

[0037]The first control unit 17 controls a single slope AD conversion, and performs the CDS. Specifically, the first control unit 17 generates a third digital signal D3 and a fourth digital signal D4, and outputs a difference between the fourth digital signal D4 and the third digital signal D3 as a fifth digital signal Dout\_l(k), based on an output signal of the edge detector 16. In addition, the first control unit 17 controls the switches RST1 and RST2.

[0038]The second control unit 18 controls a successive approximation register (SAR) AD conversion. Specifically, the second control unit 18 sets the second digital signal D and outputs the set second digital signal D as a second digital signal Dout\_m(k), based on the output signal of the edge detector 16.

[0039]The first control unit 17, the second control unit 18, and the output unit 4 function as a digital signal generation unit which generates the first digital signal Dout based on the comparison result Compo.

[0040]Subsequently, an AD conversion operation of the signal conversion unit 3(k) will be described.

[0041]FIG. 4A to FIG. 6B illustrate coupling states of the signal conversion unit 3(k) in each operation step. In FIG. 4A to FIG. 6B, configurations relating to description of the coupling states are illustrated, and other configurations are not illustrated. FIG. 7 is a timing diagram of the voltage Vpix and the third voltage Vx at the time of AD conversion operation. In FIG. 7, the ramp voltage Vramp decreases as time passes.

[0042]FIG. 4A illustrates a coupling state of the signal conversion unit 3(k) at the time of initialization (reset). FIG. 4A illustrates a coupling state from time t1 to time t2 of FIG. 7.

[0043]The second control unit 18 supplies “111” as the second digital signal D, turns on the switches S1, S3, and S5, and turns off the switches S2, S4, and S6. By doing so, the first reference voltage Vref1 is supplied to the one terminals of the first capacitors 21 to 23.

[0044]The first control unit 17 switches on the switches RST1 and RST2, in a state in which the reset voltage Vrst and the third reference voltage Vramp0 are supplied (time t1). By doing so, the reset voltage Vrst is sampled and held on the inverting input node 11b. Thus, the third voltage Vx becomes substantially the same as the reset voltage Vrst.

[0045]FIG. 4B illustrate a coupling state of the signal conversion unit 3(k) at the time of a single slope AD conversion of the reset voltage Vrst. FIG. 4B illustrates a coupling state from time t2 to time t5 of FIG. 7.

[0046]The first control unit 17 switches off the switches RST1 and RST2 (time t2). Thereafter, the first control unit 17 generates the third digital signal D3 in accordance with the elapsed time until the third voltage Vx reaches the reset voltage Vrst, in a state in which the reset voltage Vrst and the ramp voltage Vramp are supplied. As the ramp voltage Vramp decreases, the third voltage Vx decreases. In the example of FIG. 7, the elapsed time is from time t3 when the ramp voltage Vramp starts to decrease until time t4.

[0047]By doing so, noise from the pixel, an AD conversion of an offset voltage of the comparator 11 which is accumulated in the first capacitors 21 to 23, and the reset voltage Vrst involving kTC noise is performed.

[0048]Here, since there is redundancy for mismatch or the like of the first capacitors 21 to 23, the amount of changes of the ramp voltage Vramp is greater than that of the third voltage Vx which is performed by 1 LSB of the second digital signal D. A maximum value of the ramp voltage Vramp is greater than that of the third ramp voltage Vramp 0.

[0049]After time t5, the voltage Vpix changes, and after time t6, the signal voltage Vsig is supplied. A successive approximation register AD conversion is performed till time t9 after time t6.

[0050]After the third digital signal D3 is generated, the second control unit 18 successively sets each bit of the second digital signal D such that the third voltage Vx approaches the signal voltage Vsig, based on the comparison result Compo, in a state in which the signal voltage Vsig and the third reference voltage Vramp0 are supplied.

[0051]FIG. 5A illustrates a coupling state of the signal conversion unit 3(k) at the time (at the time of determining the third bit) of a successive approximation register AD conversion of the signal voltage Vsig. FIG. 5A illustrates a coupling state from time t6 to time t7 of FIG. 7.

[0052]The second control unit 18 first changes the third bit D[2] of the second digital signal D to “0”, switches off the switch S5, and switches on the switch S6 (time t6). By doing so, the third voltage Vx decreases. In the example, the decreased third voltage Vx is higher than the signal voltage Vsig.

[0053]FIG. 5B illustrates a coupling state of the signal conversion unit 3(k) at the time (at the time of judging the second bit) of a successive approximation register AD conversion of the signal voltage Vsig. FIG. 5B illustrates a coupling state from time t7 to time t8 of FIG. 7.

[0054]Since the third voltage Vx is higher than the signal voltage Vsig, the second control unit 18 sets the third bit D[2] of the second digital signal D to “0”. In addition, the second control unit 18 changes the second bit D[1] of the second digital signal D to “0”, switches off the switch S3, and switches on the switch S4 (time t7). By doing so, the third voltage Vx becomes lower than the signal voltage Vsig, in time t7, as illustrated in FIG. 7.

[0055]FIG. 6A illustrates coupling of the signal conversion unit 3(k) at the time (at the time of determining the first bit) of a successive approximation register AD conversion of the signal voltage Vsig. FIG. 6A illustrates a coupling state from time t8 to time t9 of FIG. 7.

[0056]Since the third voltage Vx is lower than the signal voltage Vsig, the second control unit 18 sets the second bit D[1] of the second digital signal D to “1”, switches on the switch S3, and switches off the switch S4 (time t8). In addition, the second control unit 18 changes the first bit D[0] of the second digital signal D to “0”, switches off the switch S1, and switches on the switch S2 (time t8). By doing so, the third voltage Vx increases, thereby becoming higher than the signal voltage Vsig, in time t8, as illustrated in FIG. 7.

[0057]FIG. 6B illustrates a coupling state of the signal conversion unit 3(k) at the time of a single slope AD conversion of the signal voltage Vsig. FIG. 6B illustrates a coupling state from time t9 to time t12 of FIG. 7.

[0058]The second control unit 18 sets the first bit D[0] of the second digital signal D to “0”. Thus, the second digital signal D is set to “010”, and is output as the second digital signal Dout\_m(k).

[0059]The first control unit 17 generates the fourth digital signal D4 in accordance with the elapsed time until the third voltage Vx reaches the signal voltage Vsig, in a state in which the second digital signal D is set and the signal voltage Vsig and the ramp voltage Vramp are supplied. In the example of FIG. 7, the elapsed time is from time t10 when the ramp voltage Vramp starts to decrease until time t11. By doing so, an AD conversion of a residual difference produced by the successive approximation register AD conversion is performed. The residual error is a difference between the third voltage Vx and the signal voltage Vsig which are obtained by performing the successive approximation register AD conversion.

[0060]The first control unit 17 outputs a difference (a value which is obtained by subtracting the fourth digital signal D4 from the third digital signal D3) between the fourth digital signal D4 and the third digital signal D3 as the fifth digital signal Dout\_l(k).

[0061]After t12, the voltage Vpix is changed, and the reset voltage Vrst of the pixel of a subsequent row is supplied. After t13, the same processing as that after t1 is performed. That is, the period from time t1 to time t13 is the same as one horizontal period (1 H) in which processing for the pixels 1 in one column is performed.

[0062]If the ramp voltage Vramp increases as time passes, the ramp voltage Vramp has a waveform illustrated in FIG. 8. In this case, the basic operation is the same as that described above. However, the first control unit 17 outputs a value obtained by subtracting the fourth digital signal D4 from the third digital signal D3 as the fifth digital signal Dout\_l(k).

[0063]FIG. 9 is a circuit diagram illustrating a configuration of the output unit 4. The output unit 4 includes a parallel-serial conversion unit 31, an offset code calculation unit 32, an SRAM 33, an offset correction unit (merging unit) 34, a gain error calculation unit 35, an SRAM 36, and a gain error correction unit 37.

[0064]The parallel-serial conversion unit 31 outputs a second digital signal Dout\_m(a) and a fifth digital signal Dout\_l(a) which corresponds to a designated column address CADD from among second digital signals Dout\_m(0) to Dout\_m(n-1) and fifth digital signals Dout\_l(0) to Dout\_l(n-1).

[0065]The offset code calculation unit 32 calculates an address in which an offset code according to the second digital signal Dout\_m(a) and the column address CADD, and supplies the calculated address to the SRAM 33.

[0066]Since the third voltage Vx includes an offset voltage between the codes of the second digital signal Dout\_m(a) due to mismatch of the first capacitors 21 to 23, the second digital signal Dout\_m(a) also includes an offset code due to the offset voltage. In order to increase accuracy of an AD conversion, it is necessary to correct the offset code. Thus, the SRAM 33 stores offset codes due to mismatch of the first capacitors 21 to 23 for each column address CADD. The SRAM 33 reads the offset code according to the address designated by the offset code calculation unit 32, and the offset code which is read to the offset correction unit 34.

[0067]The offset correction unit 34 merges the second digital signal Dout\_m(a), the fifth digital signal Dout\_l(a), and the offset code and generates the first digital signal Dout. Specifically, the first digital signal Dout is obtained by subtracting the offset code from the sum of [{11×××1 (=digital value in which 1 is aligned by the number of bits of Dout\_m(a)-second digital signal Dout\_m(a)}´2^(the number of bits of fifth digital signal Dout\_l(a))´3/4(=calculation value of Dout\_m(a))] and the fifth digital signal Dout\_l(a). The obtained first digital signal Dout represents a difference between the reset voltage Vrst and the signal voltage Vsig, but also includes a gain error.

[0068]The gain error calculation unit 35 calculates an address indicating a position in which a gain error code according to the column address CADD is stored, and supplies the calculated address to the SRAM 36.

[0069]The SRAM 36 stores the gain error code for each column address CADD. The SRAM 36 reads the gain error code according to a designated address, and supplies the gain error code which is read to the gain error correction unit 37.

[0070]The gain error correction unit 37 does arithmetic of the gain error code and the first digital signal Dout, thereby correcting the gain error included in the first digital signal Dout. The obtained first digital signal Dout represents a difference between the reset voltage Vrst and the signal voltage Vsig.

[0071]By sequentially changing the column addresses CADD, a difference between the reset voltage Vrst and the signal voltage Vsig from each pixel can be sequentially changed to the first digital signal Dout.

[0072]The offset code due to the mismatch of the first capacitors 21 to 23 is measured and is stored in the SRAM 33 in advance as follows.

[0073]FIGS. 10A to 11 illustrate coupling states of the signal conversion unit 3(k) in each operation step at the time of measuring the offset code between the first capacitors 21 and 22. In FIGS. 10A to 11, the first capacitors 21 to 23 respectively include the mismatch DC0 and DC1, or DC2. FIG. 12 is a timing diagram of the voltage Vpix and the third voltage Vx at the time of the AD conversion operation corresponding to FIGS. 10A to 11.

[0074]FIG. 10A illustrates a coupling state of the signal conversion unit 3(k) at the time of initialization (reset). FIG. 10A illustrates a coupling state which is made until time t22 of FIG. 12.

[0075]The second control unit 18 supplies “101” as the second digital signal D. By doing so, the first reference voltage Vref1 is applied to one terminal of the first capacitors 21 and 23, and the second reference voltage Vref2 is applied to one terminal of the first capacitor 22.

[0076]The first control unit 17 switches on the switches RST1 and RST2, in a state in which the reset voltage Vrst and the third reference voltage Vramp0 are supplied (time t21). By doing so, the reset voltage Vrst is sampled and held in the inverting input node 11b.

[0077]FIG. 10B illustrates coupling of the signal conversion unit 3(k) at the time of single slope AD conversion of the reference voltage. FIG. 10B illustrates a coupling state from time t22 to time t25 of FIG. 12.

[0078]The first control unit 17 switches off the switches RST1 and RST2 (time t22). Thereafter, the first control unit 17 generates the third digital signal D3 as time (from time t23 to t24) passes until the third voltage Vx reaches the reset voltage Vrst, in a state in which the reset voltage Vrst and the ramp voltage Vramp are supplied.

[0079]Subsequently, in time t26, the second control unit 18 supplies “110” as the second digital signal D. By doing so, the first reference voltage Vref1 is supplied to one terminal of the first capacitors 22 and 23, and the second reference voltage Vref2 is supplied to one terminal of the first capacitor 21. By doing so, the third voltage Vx increases to be higher than the reset voltage Vrst in time t26, as illustrated in FIG. 12.

[0080]FIG. 11 illustrates coupling of the signal conversion unit 3(k) at the time of the single slope AD conversion of a difference between the first capacitors 21 and 22. FIG. 11 illustrates a coupling state from time t27 to time t30 of FIG. 12.

[0081]The first control unit 17 generates the fourth digital signal D4 as time (from time t28 to t29) passes until the third voltage Vx reaches the reset voltage Vrst, in a state in which the ramp voltage Vramp is supplied.

[0082]A difference between the fourth digital signal D4 and the third digital signal D3 which are obtained represents a value proportional to the mismatch {C+(DC1-DC0)} between the first capacitor 22 and the first capacitor 21. A difference between the obtained difference and a difference between the fourth digital signal D4 and the third digital signal D3 which are ideal without mismatch is acquired as the offset code between the first capacitor 22 and the first capacitor 21.

[0083]Such a series of processing are repeated as follows, and thereby the offset codes are generated by the respective first capacitors 21 to 23.

[0084]FIG. 13 is a flow chart illustrating processing in which offset codes that are generated by the respective first capacitors 21 to 23 are obtained. Here, a case in which the number of the first capacitors 21 to 23 is (N+1) will be described.

[0085]First, I is set to N (step ST1).

[0086]Subsequently, the second digital signal D[N] to D[I+1] is set to “1”, D[I] is set to 0, and D[I-1] to D[0] are set to 1 (step ST2). If I=N, D[N] and D[I](=D[N]) are set to “0”.

[0087]Subsequently, AD conversion is performed, the third digital signal D3 is generated (step ST3).

[0088]Subsequently, D[N] to D[I] is set to “1”, and D[I-1] to D[0] is set to “0” (step ST4).

[0089]Subsequently, an AD conversion is performed, and thereby the fourth digital signal D4 is generated (step ST5).

[0090]Subsequently, a difference between the fourth digital signal D4 and the third digital signal D3 is calculated (step ST6). The difference is proportional to [C+{DCI-(DC(I-1)+×××+ DC0)}]. If I=0, the difference is proportional to (C+DC0).

[0091]Subsequently, if I>0 (step ST7;Yes), I=I-1 (step ST8), and the processing returns to step ST2. If I>0 is not satisfied (step ST7;No), the processing is terminated.

[0092]Offset codes corresponding to the mismatch DC0, DC1, ×××, DC(N-1), DCN can be calculated, based on (N+1) differences which are obtained in step ST6, and the calculated offset codes are stored in the SRAM 33.

[0093]Here, an AD converter according to a comparison example will be described.

[0094]FIG. 14A is a circuit diagram of an essential part of an AD converter according to a first comparison example, and FIG. 14B is a timing diagram of the AD converter.

[0095]The AD converter initially sweeps a full range using a ramp voltage Vramp\_c with a large slope, and roughly determines the voltage Vpix1 or Vpix2 (first step of FIG. 14B). Subsequently, one of a plurality of ramp voltages Vramp1 to Vramp3 with a small slope is selected, based on the determined result, and a fine single slope AD conversion of the voltage Vpix1 or Vpix2 is performed in a narrow range, using the selected ramp voltage (second step of FIG. 14B).

[0096]By doing so, it is possible to obtain a wide dynamic range, and to perform an AD conversion using a ramp voltage with a small slope. Accordingly, noise can be reduced. However, since it is necessary to generate a plurality of ramp voltages Vramp1 to Vramp3, an area and power increase.

[0097]FIG. 15A is a circuit diagram of an essential part of an AD converter according to a second comparison example, and FIG. 15B is a timing diagram of the AD converter.

[0098]The AD converter initially samples and holds the voltage Vpix in a DAC 14X of a capacitor type by switching on the switch Sx only for a predetermined period, and successively sets each bits of a digital signal, while performing a successive approximation register operation of the voltage VA and the reference voltage Vref1 (until time t1x). Subsequently, a single slope AD conversion of a voltage VA of a residual difference is performed by using the ramp voltage Vramp (after time t1x). Finally, a digital signal which is set by the successive approximation register is merged with a digital signal which is generated by the single slope AD conversion, and thereby a digital signal corresponding to the voltage Vpix is obtained. The AD conversion operation is performed in both a case in which the voltage Vpix is the reset voltage Vrst and a case in which the voltage Vpix is the signal voltage Vsig, and a difference between the obtained two digital signals is obtained (CDS).

[0099]In the configuration, it is possible to obtain a wide dynamic range and to reduce noise. In addition, since only one ramp voltage Vramp may be generated, it is possible to further reduce an area and power, compared to the first comparison example.

[0100]However, when the reset voltage Vrst is sampled and held, and when the signal voltage Vsig is sampled and held, kTC noises Vn\_rst and Vn\_sig which have no correlation with each other are retained in a capacitor of the DAC 14X of a capacitor type. For this reason, as illustrated in FIG. 16A, even though a difference between a digital signal AD[Vrst+Vn\_rst] which is obtained by performing an AD conversion of the reset voltage Vrst and a digital signal AD[Vsig+Vn\_sig] which is obtained by performing an AD conversion of the signal voltage Vsig is taken, the kTC noises Vn\_rst and Vn\_sig cannot be cancelled, and the noise increases more than that in the first comparison example. In order to reduce the kTC noises, it is necessary to increase a value of the capacitor of the DAC 14X of a capacitor type.

[0101]In contrast to this, in the present embodiment, the reset voltage Vrst or the signal voltage Vsig are supplied to the non-inverting input node 11a of the comparator 11. Then, the switches RST1 and RST2 are switched on, and thereby the reset voltage Vrst is sampled and held in the capacitor unit 14 coupled to the inverting input node 11b. An AD conversion of the signal voltage Vsig is performed by making the reset voltage Vrst which is sampled and held in the capacitor unit 14 approach the signal voltage Vsig, without sampling and holding of the signal voltage Vsig. That is, while AD conversion of a difference between the reset voltage Vrst and the signal voltage Vsig into the first digital signal Dout is performed, the kTC noise Vn\_rst is sampled and held only once at the time of sampling and holding of the reset voltage Vrst.

[0102]For this reason, the kTC noise Vn\_rst which is included in the third digital signal D3 based on the reset voltage Vrst is the same as the kTC noise Vn\_rst which is included in the fourth digital signal D4 based on the signal voltage Vsig. Thus, by taking a difference between the fourth digital signal D4 and the third digital signal D3, the kTC noise Vn\_rst is cancelled (FIG. 16B). Accordingly, in the present embodiment, the noise of the first digital signal Dout can be reduced by the kTC noise, compared to the second comparison example.

[0103]In addition, since only one ramp voltage may be generated, it is possible to reduce an area and power further than those in the first comparison example. Accordingly, it is possible to perform an AD conversion with a small area, a wide dynamic range, and low noise.

Second Embodiment

[0104]In a second embodiment, an operation point of the comparator 11 is constant.

[0105]FIG. 17 is a circuit diagram illustrating a configuration of a signal conversion unit 3A(k) according to the second embodiment. In FIG. 17, the same symbols or reference numerals are attached to the same configuration elements as those of FIG. 3 according to the first embodiment, and hereinafter, a difference between those will be mainly described.

[0106]The signal conversion unit 3A(k) includes an input capacitor 19 and a second switch RST3, in addition to the configuration of FIG. 3. The comparator 12, the capacitor 13, the switch RST2, the edge detector 16, the first control unit 17, and the second control unit 18 are not illustrated in FIG. 17.

[0107]The input capacitor 19 has one terminal to which the reset voltage Vrst or the signal voltage Vsig is supplied as the voltage Vpix.

[0108]The inverting input node (first input node) 11b of the comparator 11 is coupled to the other terminal of the input capacitor 19. The comparator 11 compares a third voltage Vy of the inverting input node 11b to a fourth voltage Vx of the non-inverting input node (second input node) 11a, and outputs the comparison result.

[0109]The second switch RST3 is coupled between the non-inverting input node 11a and a reference voltage node N1 to which a fourth reference voltage Vref3 is supplied.

[0110]One terminal of each of the first capacitors 21 to 23 and the second capacitor 15 is coupled to the non-inverting input node 11a.

[0111]In a state in which the reset voltage Vrst and the third reference voltage Vramp0 are supplied, the first control unit 17 switches on the first and second switches RST1 to RST3, and thereafter switches off the first and second switches RST1 to RST3. By doing so, the fourth reference voltage Vref3 is sampled and held in the capacitor unit 14. Thereafter, in a state in which the reset voltage Vrst and the ramp voltage Vramp are supplied, the first control unit 17 generates the third digital signal D3 as time passes until the fourth voltage Vx reaches the third voltage Vy.

[0112]After the third digital signal D3 is generated, the second control unit 18 successively sets each bit of the second digital signal D such that the fourth voltage Vx approaches the third voltage Vy, in a state in which the signal voltage Vsig and the third reference voltage Vramp0 are supplied.

[0113]Then, in a state in which the second digital signal D is set and the signal voltage Vsig and the ramp voltage Vramp are supplied, the first control unit 17 generates the fourth digital signal D4 as time passes until the fourth voltage Vx reaches the third voltage Vy.

[0114]The other operations are the same as those in the first embodiment.

[0115]In the first embodiment, the reset voltage Vrst is sampled and held at the time of initialization, and thus the reset voltage Vrst becomes an operation point of the comparator 11. The reset voltage Vrst differs for each pixel due to mismatch of the pixels. For this reason, there is a probability that an operation point of the comparator 11 and characteristics of the comparator 11 are changed for each pixel which is measured. Due to this, accuracy of an AD conversion can be reduced.

[0116]Meanwhile, according to the present embodiment, the fourth reference voltage Vref3 is sampled and held at the time of initialization, and thus the operation point of the comparator 11 can be constant, regardless of the reset voltage Vrst. Accordingly, characteristics of the comparator 11 can be constant regardless of the pixels 1 to be measured, and thus it is possible to increase accuracy of an AD conversion.

Third Embodiment

[0117]In a third embodiment, a plurality of single slope AD conversions is performed by using the ramp voltage Vramp which is supplied multiple times.

[0118]FIG. 18 is a circuit diagram illustrating a configuration of a signal conversion unit 3B(k) according to the third embodiment. In FIG. 18, the same symbols or reference numerals are attached to the same configuration elements as those of FIG. 3 according to the first embodiment, and hereinafter, a difference between those will be mainly described.

[0119]The signal conversion unit 3B(k) further includes a setting unit 41 in addition to the configuration of FIG. 3. A first control unit 17B, the second control unit 18, the setting unit 41, and the output unit 4 function as a digital signal generation unit. In addition, the ramp voltage Vramp is supplied 2M times (M is an integer larger than or equal to “1”). Hereinafter, an example of M=2 will be described.

[0120]FIG. 19 is a timing diagram of the voltage Vpix and the third voltage Vx at the time of an AD conversion operation.

[0121]An operation until time t41 is the same as that in the first embodiment.

[0122]The ramp voltages Vramp having the same level are repeatedly supplied four times, during a period from time t41 to time t42. If the ramp voltage Vramp is supplied multiple times in a state in which the reset voltage Vrst is supplied, the first control unit 17B generates the third digital signal D3 multiple times. Whenever the ramp voltage Vramp is supplied, the first control unit 17B generates the third digital signal D3 in the same manner as in the first embodiment. Accordingly, the third digital signal D3 is generated four times.

[0123]After time t43, the signal voltage Vsig is supplied. FIG. 19 illustrates a dark time when the signal voltage Vsig similar to the reset voltage Vrst is supplied, and a bright time when the signal voltage Vsig lower than the signal voltage Vsig at the dark time is supplied.

[0124]During a period from time t43 to time t44, the second control unit 18 sets the second digital signal D according to the successive approximation register AD conversion, in the same manner as in the first embodiment. In time t44, for example, the second digital signal D at the dark time is set to “111”, and the second digital signal D at the bright time is set to “001”.

[0125]During a period from time t45 to t47, the ramp voltages Vramp having the same level are repeatedly supplied four times. After the second digital signal D is set, if the ramp voltage Vramp is supplied multiple times in a state in which the signal voltage Vsig is supplied, the first control unit 17B generates the fourth digital signal D4 by the number of generations which is determined by the second digital signal D. Whenever the ramp voltage Vramp is supplied, the first control unit 17B generates the fourth digital signal D4 in the same manner as in the first embodiment.

[0126]The greater a difference between the reset voltage Vrst and the signal voltage Vsig is, the smaller the number of generations is set by the setting unit 41, and the greater the amount of shifts is set by the setting unit 41 in response to the second digital signal D. The setting unit 41 retains a correspondence relationship as illustrated in FIG. 20A. FIG. 20A illustrates a correspondence relationship between the second digital signal D, the number of generations, and the amount of shifts. If M=2, the number of generations at the dark time (D=”111”) is four, and the number of generations at the bright time (D=”001”) is one (not illustrated).

[0127]By doing so, during a period from time t45 to time t47, the fourth digital signal D4 is generated four times at the dark time, and the fourth digital signal D4 is generated once at the bright time. At the dark time in which requirements with respect to random noise is strict, the fourth digital signal D4 is generated four times, and thereby the random noise can be reduced. At the bright time, shot noise is dominant, and thus requirements with respect to the random noise are loose. For this reason, by generating the fourth digital signal D4 once or by the number of times smaller than that at the dark time, it is possible to reduce power consumption.

[0128]The first control unit 17B includes a counter 42 which counts the elapsed time. After the fourth digital signal D4 is generated by the number of generations, the first control unit 17B stops operations of the counter 42 and the comparators 11 and 12. In a case of a bright time, during a period from time t46 to t47 after the fourth digital signal D4 is generated once, the third voltage Vx is changed in accordance with the ramp voltage Vramp, but the counter 42 and the comparators 11 and 12 do not operate, and thereby power consumption can be reduced.

[0129]Thereafter, the first control unit 17B outputs a difference (value which is obtained by subtracting the sum of bits of the third digital signal D3 from the sum of bits of the fourth digital signal D4) between the sum of bits of the fourth digital signal D4 and the sum of bits of the third digital signal D3 as the fifth digital signal Dout\_l(k).

[0130]In the same manner as in the first embodiment, the offset correction unit 34 generates the first digital signal Dout by merging the second digital signal Dout\_m(k), the fifth digital signal Dout\_l(k), and the offset code.

[0131]The number of single slope AD conversions of the reset voltage Vrst is greater than the number of single slope AD conversions of the signal voltage Vsig at the bright time. For this reason, the number of summed bits of the third digital signal D3 is greater than the number of bits of the fourth digital signal D4 at the bright time. Thus, processing for equalizing the number of bits is performed.

[0132]The first control unit 17B reduces the number of summed bits of the third digital signal D3 by the shifted amount of bits determined by the second digital signal D. The shifted amount of bits is set in accordance with the correspondence relationship of FIG. 20A. The number of summed bits of the third digital signal D3 whose number of bits are reduced is equal to the number of summed bits of the fourth digital signal D4.

[0133]The first control unit 17B increases the number of bits of a difference (a value which is obtained by subtracting the sum of bits of the third digital signal D3 whose number of bits is reduced from the sum of bits of the fourth digital signal D4) between the sum of bits of the fourth digital signal D4 and the sum of bits of the third digital signal D3 whose number of bits is reduced, by the shifted amount of bits, and outputs a difference in which the number of bits is increased, as the fifth digital signal Dout\_l(k). The processing for increasing the number of bits may be performed by the output unit 4.

[0134]FIG. 20B illustrates an example in which bits are shifted in a case in which M=2.

[0135]In the example, the third digital signal D3 and the fourth digital signal D4 which are generated once respectively have eight bits. Thus, the sum of bits of four third digital signals D3 is 10 bits.

[0136]At the dark time (D=”111”), the sum of bits of four fourth digital signals D4 is 10 bits. The shifted amount of bits is zero. Thus, a difference (CDS result) between the sum of bits of the fourth digital signal D4 with 10 bits and the sum of bits of the third digital signal D3 with 10 bits is 10 bits.

[0137] At the dark time (D=”000”), the fourth digital signal D4 is generated once. The shifted amount of bits is 2. Thus, the sum of bits of the third digital signal D3 with 10 bits is shifted to the right by two bits, thereby being eight bits. That is, two bits from the lowest level of the sum of bits of the third digital signal D3 are deleted.

[0138]Accordingly, a difference (CDS result) between the sum of bits of the fourth digital signal D4 with eight bits and the sum of bits of the third digital signal D3 with eight bits is eight bits.

[0139]Finally, the above-described difference is shifted to the left by two bits, thereby being 10 bits. That is, two bits from the lowest level of the above-described difference become “00”. By doing so, it is possible to obtain the appropriate fifth digital signal Dout\_l(k), also at the bright time.

[0140] In this way, in the present embodiment, the single slope AD conversion is performed multiple times, and thus it is possible to further reduce the noise than that in the first embodiment.

[0141]In addition, the number of supplying of the ramp voltage Vramp can be arbitrarily set within a range in one horizontal period, and thus an adjustment range of the amount of noise to be reduced is widened.

Fourth Embodiment

[0142]In a fourth embodiment, the single slope AD conversion is performed multiple times by dividing a first capacitor 23C into unit capacitors 25 and 26 and switching voltages which are supplied to the unit capacitors 25 and 26.

[0143]FIG. 21 is a circuit diagram illustrating a configuration of a signal conversion unit 3C(k) according to a fourth embodiment. In FIG. 21, the same symbols or reference numerals are attached to the same configuration elements as those of FIG. 18 according to the third embodiment, and hereinafter, a difference between those will be mainly described. The comparator 12, the capacitor 13, the switch RST2, the edge detector 16, the first control unit 17B, the second control unit 18, and the setting unit 41 are not illustrated in FIG. 21.

[0144]A capacitor unit 14C further includes a first capacitor 24 (capacitance value 8C). That is, the second digital signal D has four bits. A first capacitor 23C having a capacitance value 4C which is quadruple a unit capacitance value C is divided into two unit capacitors 25 and 26 which respectively have a capacitance value 2C that is double the unit capacitance value C. A first capacitor 23C corresponds to the capacitor 23 of FIG. 18.

[0145]Each of the unit capacitors 25 and 26 has one terminal coupled to the inverting input node 11b, and the other terminal to which the first reference voltage Vref1 and the second reference voltage Vref2 are supplied.

[0146]Each of switches S5 and S7 has one terminal coupled to the other terminal of the corresponding unit capacitor, and the other terminal to which the first reference voltage Vref1 is supplied. Each of switches S6 and S8 has one terminal coupled to the other terminal of the corresponding unit capacitor, and the other terminal to which the second reference voltage Vref2 is supplied.

[0147]A switch S9 has one terminal coupled to the other terminal of a capacitor 24, and the other terminal to which the first reference voltage Vref1 is supplied. A switch S10 has one terminal coupled to the other terminal of the capacitor 24, and the other terminal to which the second reference voltage Vref2 is supplied.

[0148]FIGS. 22A and 22B and FIGS. 23A and 23B illustrate coupling states of a signal conversion unit 3C(k) in each operation step of the single slope AD conversion. FIG. 24 is a timing diagram of the voltage Vpix and the third voltage Vx at the time of AD conversion operation.

[0149]FIG. 22A illustrates a coupling state of the signal conversion unit 3C(k) at the time of the first single slope AD conversion. FIG. 22A illustrates a coupling state during a period from time t51 to time t52 of FIG. 24.

[0150]The ramp voltage Vramp (not illustrated) starts to increase after time t51, and increases monotonically and continuously until time t55. That is, the ramp voltage Vramp is supplied once during this period. A minimum value of the ramp voltage Vramp is less than the third reference voltage Vramp0.

[0151]The first reference voltage Vref1 is supplied to one terminal of each of the first capacitors 21, 22, and 24 and the unit capacitors 25 and 26. An operation until time t52 is the same as that in the third embodiment, and thereby third digital signal D3 is generated.

[0152]In a state in which the reset voltage Vrst and the ramp voltage Vramp are supplied, and after the third digital signal D3 is generated, the first control unit 17B performs processing for switching a voltage which is supplied to the other terminal of any one of the unit capacitors 25 and 26 and the first capacitor 22, and generating the third digital signal D3, once or more (here, thrice).

[0153]FIG. 22B illustrates a coupling state of the signal conversion unit 3C(k) at the time of the second single slope AD conversion. FIG. 22B illustrates a coupling state during a period from time t52 to time t53 of FIG. 24.

[0154]At time t52, a voltage which is supplied to the first capacitor 22 is switched to the second reference voltage Vref2 less than the first reference voltage Vref1, and the third voltage Vx decreases. At time t52, the decreased third voltage Vx is substantially equal to the third voltage Vx shortly before an increase after time t51. Since the third voltage Vx becomes lower than the reset voltage Vrst again, it is possible to perform again the single slope AD conversion according to an increase (that is, an increase of the third voltage Vx) of the ramp voltage Vramp.

[0155]FIG. 23A illustrates a coupling state of the signal conversion unit 3C(k) at the time of the third single slope AD conversion. FIG. 23A illustrates a coupling state during a period from time t53 to time t54 of FIG. 24.

[0156]At time t53, a voltage which is supplied to the unit capacitor 25 is switched to the second reference voltage Vref2, and the third voltage Vx decreases. Since a capacitance value of the unit capacitor 25 is substantially equal to a capacitance value of the first capacitor 22, the third voltage Vx which is decreased in time t53 is substantially equal to the third voltage Vx shortly before an increase after time t51. As a result, it is possible to perform the single slope AD conversion again.

[0157]FIG. 23B illustrates a coupling state of the signal conversion unit 3C(k) at the time of the fourth single slope AD conversion. FIG. 23B illustrates a coupling state during a period from time t54 to time t55 of FIG. 24.

[0158]At time t54, a voltage which is supplied to the unit capacitor 26 is switched to the second reference voltage Vref2, and the third voltage Vx decreases. As a result, it is possible to perform the single slope AD conversion again.

[0159]By doing so, the single slope AD conversion is performed four times while one ramp voltage Vramp is supplied, and four third digital signal D3 can be generated. At time t55, the first reference voltage Vref1 is supplied to the first capacitor 22 and the unit capacitors 25 and 26 again.

[0160]After time t56, the signal voltage Vsig is supplied, and the successive approximation register AD conversion is performed until time t57. At this time, the switches S5 and S7 are controlled in the same state as each other, and the switches S6 and S8 are controlled in the same state as each other. By doing so, in the same manner as in the third embodiment, the first reference voltage Vref1 or the second reference voltage Vref2 is supplied to the other terminal of the capacitor 23C with a capacitance value 4C. Accordingly, the successive approximation register AD conversion is performed in the same manner as in the third embodiment. In this way, the unit capacitors 25 and 26 are used for both a level shift and the successive approximation register AD conversion.

[0161]In the example which is illustrated, the second digital signal D is set to “1111” at the dark time, and the second digital signal D is set to “0001” at the bright time.

[0162]After the second digital signal D is set by the successive approximation register AD conversion, the first control unit 17B generates the fourth digital signal D4 by the number of generations which is determined by the second digital signal D. The number (number of generations) of the single slope AD conversion is determined by the second digital signal D which is set. For example, if the second digital signal D is “0000”, the second reference voltage Vref2 is supplied to the unit capacitors 25 and 26 and the first capacitor 22. Thus, even though the switches S3 to S8 are switched, it is not possible to decrease the third voltage Vx, and thus the single slope AD conversion is performed only once. For this reason, the number of generations is set in accordance with, for example, the correspondence relationship of FIG. 25.

[0163]FIG. 25 illustrates a correspondence relationship between the second digital signal D, the number of generations, and the amount of shifted bits. The number of generations at the dark time (D=”1111”) is four, and the number of generations at the bright time (D=”0001”) is one.

[0164]If the number of generations is multiple, the first control unit 17B, in a state in which the signal voltage Vsig and the ramp voltage Vramp are supplied, after the fourth digital signal D4 is generated, the first control unit 17B performs processing for switching a voltage which is supplied to the other terminal of any one of the unit capacitors 25 and 26 and the first capacitor 22, and generating the fourth digital signal D4 once or more.

[0165]The ramp voltage Vramp (not illustrated) starts to increase after time t58, and increases continuously and monotonically until time t60. That is, the ramp voltage Vramp is supplied only once during this period.

[0166]At the dark time (D=”1111”), the single slope AD conversion is performed four times from time t58 to time t60, and the fourth digital signal D4 is generated four times. The operation at this time is the same from time t51 to t55.

[0167]At the bright time (D=”0001”), the single slope AD conversion is performed once from time t58 to t59, and the fourth digital signal D4 is generated once. During a period from time t59 after that until time t60, the counter 42 and the comparators 11 and 12 are stopped, and thereby it is possible to reduce power consumption. The voltage which is supplied to the other terminal of the unit capacitors 25 and 26 and the first capacitor 22 may also not be switched. A portion of the waveform of the third voltage Vx from time t59 to time t60 is not illustrated.

[0168]Thereafter, in the same manner as in the third embodiment, adjustment of the number of bits at the bright time, CDS, and mergence are performed, and the first digital signal Dout is generated.

[0169]FIG. 26 illustrates a relationship between the amount of the third voltage Vx shifted by the unit capacitors 25 and 26 and the amount of the third voltage Vx changed by 1 LSB of the second digital signal D. The amount of the third voltage Vx shifted by the unit capacitors 25 and 26 is double the amount of the third voltage Vx changed by 1 LSB of the second digital signal D. As a result, there is redundancy for mismatch or the like of the first capacitors 21, 22, 23C, and 24, and the single slope AD conversion can be reliably performed.

[0170]According to the present embodiment, in the same manner as in the third embodiment, the single slope AD conversion is performed multiple times, and thus noise can be reduced.

[0171]In addition, since one first capacitor 23C is divided into a plurality of unit capacitors 25 and 26 and a capacitor is not added, it is possible to have the same area as that in the third embodiment.

[0172]In addition, it is possible to perform multiple times the single slope AD conversion in a short time, and to linearly increase the third voltage Vx, compared to the third embodiment.

[0173]In the third embodiment, when a ramp voltage generation circuit (not illustrated) supplies the ramp voltage Vramp multiple times, it is necessary to stand by for a predetermined time, when a certain ramp voltage Vramp is switched to another ramp voltage Vramp by characteristics of the ramp voltage generation circuit (refer to FIG. 19). For this reason, in order to perform the single slope AD conversion by the same number of times, a longer time than the present embodiment is required. In addition, in the third embodiment, if a subsequent ramp voltage Vramp is supplied without standing by for enough time, the ramp voltage Vramp is non-linearized by characteristics of a ramp voltage generation circuit. Thus, the third voltage Vx non-linearly increases, and accuracy of the AD conversion can be degraded.

[0174]An example in which the first capacitor 23C having a capacitance value of 4C is divided ino the unit capacitors 25 and 26 is described, but if the first capacitor 24 having a capacitance value of 8C is also divided into four unit capacitors, the single slope AD conversion can be performed eight times. In addition, the first capacitor having a larger capacitance value is provided, and the first capacitor may be divided into unit capacitors. That is, at least one of the first capacitors having capacitance values which are quadruple or more the unit capacitance C may include a plurality of unit capacitors, each having a capacitance value which is double the unit capacitance C. The number of unit capacitors may be determined in accordance with trade-off between noise and an area which are targeted.

[0175]In addition, the first capacitor 24 may not be provided.

[0176]In addition, when the single slope AD conversion is performed multiple times, a sequence of switching voltages which are supplied to the first capacitor 22 and the unit capacitors 25 and 26 is not limited in particular.

Fifth Embodiment

[0177]In a fifth embodiment, a third capacitor 28 for level shift is added, and a voltage which is supplied to the third capacitor 28 is switched. Accordingly, the single slope AD conversion is performed multiple times.

[0178]FIG. 27 is a circuit diagram illustrating a configuration of a signal conversion unit 3D(k) according to a fifth embodiment. In FIG. 27, the same symbols or reference numerals are attached to the same configuration elements as those of FIG. 18, and hereinafter, a difference between those will be mainly described. The comparator 12, the capacitor 13, the switch RST2, the edge detector 16, the first control unit 17B, the second control unit 18, and the setting unit 41 are not illustrated in FIG. 27.

[0179]The signal conversion unit 3D(k) further includes the third capacitor 28, and switches S7 and S8. The third capacitor 28 has one terminal coupled to the inverting input node 11b and the other terminal to which the first reference voltage Vref1 and the second reference voltage Vref2 are supplied. A capacitance value of the third capacitor 28 is aC (a is a number greater than “1”).

[0180]The switch S7 has one terminal coupled to the other terminal of the third capacitor 28 and the other terminal to which the first reference voltage Vref1 is supplied. The switch S8 has one terminal coupled to the other terminal of the third capacitor 28 and the other terminal to which the second reference voltage Vref2 is supplied.

[0181]Here, an example in which one third capacitor 28 is included is described, but a plurality of third capacitors 28 may be included. In this case, each of the plurality of third capacitors 28 has one terminal coupled to the inverting input node 11b and the other terminal to which the first reference voltage Vref1 or the second reference voltage Vref2 is supplied. A capacitance value of each of the third capacitors 28 is greater than the unit capacitance value C. The greater number of the third capacitors 28 is, the more the number of single slope AD conversions can be increased.

[0182]FIG. 28 is a timing diagram of the voltage Vpix and the third voltage Vx at the time of an AD conversion operation. A difference between the fifth embodiment and the third embodiment will be mainly described.

[0183]The ramp voltage Vramp (not illustrated) starts to decrease after time t61, and decreases monotonically and continuously until time t63. An operation until time t62 is the same as that in the third embodiment, and thereby third digital signal D3 is generated. During the period, the second reference voltage Vref2 is supplied to the third capacitor 28.

[0184]In a state in which the reset voltage Vrst and the ramp voltage Vramp are supplied, and after the third digital signal D3 is generated, the first control unit 17B performs processing for switching a voltage which is supplied to the other terminal of any one of the third capacitors 28, and generating the third digital signal D3, once or more (here, once).

[0185]That is, in time t62, a voltage which is supplied to the third capacitor 28 is switched to the first reference voltage Vref1 higher than the second reference voltage Vref2, the third voltage Vx is increased, and the single slope AD conversion is performed again.

[0186]By doing so, while one ramp voltage Vramp is supplied, the single slope AD conversion is performed twice, and it is possible to generate two third digital signals D3. In time t63, the first reference voltage Vref1 is supplied to the third capacitor 28 again.

[0187]After time t64, the signal voltage Vsig is supplied, and until time t65, the successive approximation register AD conversion is performed and the second digital signal D is set. During the successive approximation register AD conversion, the voltage which is supplied to the third capacitor 28 is not switched.

[0188]The ramp voltage Vramp (not illustrated) starts to decrease until time t66, and decreases monotonically and continuously until time t68.

[0189]After the second digital signal D is set, the first control unit 17B generates the fourth digital signal D4 by the number of generations which is determined by the second digital signal D. If the number of generations is multiple, in a state in which the signal voltage Vsig and the ramp voltage Vramp are supplied, the first control unit 17B performs processing for generating the fourth digital signal D4, switching the voltage which is supplied to the other terminal of any one of the third capacitors 28, and generating the fourth digital signal D4, once or more (here, once).

[0190]At the dark time (D=”111”), the single slope AD conversion is performed twice, and the fourth digital signal D4 is generated twice until time t68 after time t66. The operation at this time is the same as that from time t61 to time t63.

[0191]At the bright time (D=”001”), the single slope AD conversion is performed once, and the fourth digital signal D4 is generated once until time t67 after time t66. During a period from time t67 to time t68, the counter 42 and the comparators 11 and 12 are stopped. The voltage which is supplied to the other terminal of the third capacitor 28 may also not be switched.

[0192]Thereafter, in the same manner as in the third embodiment, adjustment of the number of bits at the bright time, CDS, and mergence are performed, and the first digital signal Dout is generated.

[0193]FIG. 29 illustrates a relationship between the amount of the third voltage Vx shifted by the third capacitor 28 and the amount of the third voltage Vx changed by 1 LSB of the second digital signal D. Since a capacitance value of the third capacitor 28 is aC, the amount of the third voltage Vx shifted by the third capacitor 28 is a times the amount of the third voltage Vx changed by 1 LSB of the second digital signal D. As a result, there is redundancy for mismatch or the like of the first capacitors 21 to 23, and the single slope AD conversion can be reliably performed.

[0194]According to the present embodiment, the same effects as those in the fourth embodiment are obtained.

[0195]The second embodiment may be combined with the third to fifth embodiments.

[0196]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a comparator that includes a first input node to which a first voltage or a second voltage is supplied, a second input node to which a third voltage is supplied, and an output node, and that outputs a comparison result which is obtained by comparing the first voltage or the second voltage to the third voltage from the output node;

a capacitor unit that includes a plurality of first capacitors, each having one terminal which is coupled to the second input node, and the other terminal to which a first reference voltage or a second reference voltage is supplied;

a second capacitor that includes one terminal to which a third reference voltage or a ramp voltage is supplied, and the other terminal which is coupled to the second input node;

a switch that is coupled between the second input node and the output node; and

a digital signal generation unit that generates a first digital signal based on the comparison result.

2. A semiconductor integrated circuit comprising:

an input capacitor having one terminal to which a first voltage or a second voltage is supplied;

a comparator that includes a first input node which is coupled to the other terminal of the input capacitor, a second input node, and an output node, and that outputs a comparison result which is obtained by comparing a third voltage of the first input node to a fourth voltage of the second input node from the output node;

a capacitor unit that includes a plurality of first capacitors, each having one terminal which is coupled to the second input node, and the other terminal to which a first reference voltage or a second reference voltage is supplied;

a second capacitor that includes one terminal to which a third reference voltage or a ramp voltage is supplied, and the other terminal which is coupled to the second input node;

a first switch which is coupled between the first input node and the output node;

a second switch that is coupled between the second input node and a reference voltage node to which a fourth reference voltage is supplied; and

a digital signal generation unit that generates a first digital signal based on the comparison result.

3. The semiconductor integrated circuit according to Claim 1 or 2,

wherein capacitance values of the plurality of first capacitors are weighted to a product of a unit capacitance value and a power of 2,

wherein at least one of the first capacitors having capacitance values which are quadruple the unit capacitance value, includes a plurality of unit capacitors, each having a capacitance value which is double the unit capacitance value, and

wherein each unit capacitor includes one terminal which is coupled to the second input node, and the other terminal to which the first reference voltage or the second reference voltage is supplied.

4. The circuit according to any one of Claims 1 to 3,

wherein the first voltage is a reset voltage when a pixel of an image sensor is not irradiated with light, and

wherein the second voltage is a signal voltage when the pixel is irradiated with light.

5. An image sensor comprising:

a pixel; and

an AD converter which converts a difference between a reset voltage when the pixel is not irradiated with light, and a signal voltage when the pixel is irradiated with light into a digital signal,

wherein the AD converter includes:

a comparator that includes a first input node to which the reset voltage or the signal voltage is supplied, a second input node, and an output node, and that outputs a comparison result which is obtained by comparing a voltage of the first input node to a voltage of the second input node from the output node;

a capacitor unit that includes a plurality of first capacitors, each having one terminal which is coupled to the second input node, and the other terminal to which a first reference voltage or a second reference voltage is supplied;

a second capacitor that includes one terminal to which a third reference voltage or a ramp voltage is supplied, and the other terminal which is coupled to the second input node;

a switch that is coupled between the second input node and the output node; and

a digital signal generation unit that generates the digital signal based on the comparison result.

ABSTRACT

According to an embodiment, a semiconductor integrated circuit includes a comparator, a capacitor unit having a plurality of first capacitors, a second capacitor, a switch, and a digital signal generation unit. The comparator outputs a comparison result which is obtained by comparing a first voltage or a second voltage of a first input node to a third voltage of a second input node from the output node. The plurality of first capacitors respectively have one terminal which is coupled to the second input node and the other terminal to which a first reference voltage or a second reference voltage is supplied. The second capacitor includes one terminal to which a third reference voltage or a ramp voltage is supplied, and the other terminal which is coupled to the second input node. The switch is coupled between the second input node and the output node. The digital signal generation unit generates a first digital signal based on the comparison result.

Drawings

FIG. 4A

RESET

FIG. 4B

RESET VOLTAGE AD CONVERSION

FIG. 5A

SIGNAL VOLTAGE SAR

FIG. 5B

SIGNAL VOLTAGE SAR

FIG. 6A

SIGNAL VOLTAGE SAR

FIG. 6B

SIGNAL VOLTAGE AD CONVERSION

FIG. 7

VOLTAGE

TIME

FIG. 4A

FIG. 4B

FIG. 5A

FIG. 5B

FIG. 6A

FIG. 6B

FIG. 8

VOLTAGE

TIME

FIG. 4A

FIG. 4B

FIG. 5A

FIG. 5B

FIG. 6A

FIG. 6B

FIG. 9

34: OFFSET CORRECTION UNIT

32: OFFSET CODE CALCULATION UNIT

37: GAIN ERROR CORRECTION UNIT

35: GAIN ERROR CALCULATION UNIT

FIG. 12

VOLTAGE

TIME

FIG. 10A

FIG. 10B

FIG. 11

FIG. 13

ST6: CALCULATE DIFFERENCE BETWEEN FOURTH DIGITAL SIGNAL AND THIRD DIGITAL SIGNAL

FIG. 14A

FIRST COMPARISON EXAMPLE

FIG. 14B

VOLTAGE

TIME

FIRST STEP

SECOND STEP

FIG. 15A

SECOND COMPARISON EXAMPLE

FIG. 15B

VOLTAGE

TIME

SAR OPERATION

SS OPERATION

FIG. 16A

SECOND COMPARISON EXAMPLE

WHEN SAMPLING RESET VOLTAGE

WHEN SAMPLING SIGNAL VOLTAGE

FIG. 16B

FIRST EMBODIMENT

WHEN SAMPLING RESET VOLTAGE

FIG. 19

VOLTAGE

DARK TIME

BRIGHT TIME

TIME

FIG. 20A

SECOND DIGITAL SIGNAL D

NUMBER OF GENERATIONS

AMOUNT OF SHIFTED BITS

FIG. 20B

IF M=2

SUM OF D3

SUM OF D4

CDS RESULT

SUM OF D3

CDS RESULT

FIG. 24

VOLTAGE

DARK TIME

BRIGHT TIME

TIME

FIG. 25

SECOND DIGITAL SIGNAL D

NUMBER OF GENERATIONS

AMOUNT OF SHIFTED BITS

FIG. 26

VOLTAGE

SAR OF 1 LSB

SAR OF 2 LSB

TIME

FIG. 28

VOLTAGE

DARK TIME

BRIGHT TIME

TIME

FIG. 29

VOLTAGE

TIME